

WHAT IS CLAIMED IS:

1 1. A semiconductor device, comprising:
2 a semiconductor substrate having source and drain regions located therein and
3 having similar doping profiles;
4 a channel region extending from said source region to said drain region;
5 a dielectric layer located over said source and drain regions and having first and
6 second thicknesses wherein said second thickness is substantially less than said first
7 thickness and is partially located over said channel region; and
8 a gate located over said dielectric layer wherein said second thickness is located
9 between an end of said gate and one of said source and drain regions.

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11 2. The semiconductor device recited in Claim 1 wherein said first thickness
12 ranges between about 25 nm to about 50 nm.

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14 3. The semiconductor device recited in Claim 1 wherein said second
15 thickness ranges between about 6 nm and about 20 nm.

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17 4. The semiconductor device recited in Claim 1 wherein said dielectric layer
18 includes an interface between first and second layers thereof.

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20 5. The semiconductor device recited in Claim 1 wherein said doping profiles
21 of said source and drain regions include a doping concentration of about $1.0E20$
22 atoms/cm³.

1 6. The semiconductor device recited in Claim 1 wherein said source and
2 drain regions each include a lightly doped region, wherein said end of said gate and
3 said second thickness are located over one of said lightly doped regions.

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5 7. The semiconductor device recited in Claim 6 wherein said lightly doped
6 regions have a doping concentration ranging between about $1.0E17$ atoms/cm³ and
7 about $1.0E18$ atoms/cm³.

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9 8. The semiconductor device recited in Claim 1 wherein said gate is a
10 floating gate and said device further includes a control gate located over said floating
11 gate.

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13 9. The semiconductor device recited in Claim 1 wherein a coupling ratio of
14 said semiconductor device is at least about 0.7.

1 10. A method of manufacturing a semiconductor device, comprising:
2 implanting source and drain regions having similar doping profiles in a
3 semiconductor substrate, thereby defining a channel region extending from said source
4 region to said drain region;
5 locating a dielectric layer over said source and drain regions, said dielectric layer
6 having first and second thicknesses wherein said second thickness is substantially less
7 than said first thickness and is partially located over said channel region; and
8 forming a gate over said dielectric layer wherein said second thickness is located
9 between an end of said gate and one of said source and drain regions.

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11 11. The method recited in Claim 10 wherein said implanting includes
12 implanting said source and drain regions simultaneously.

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14 12. The method recited in Claim 10 wherein said first thickness ranges
15 between about 25 nm to about 50 nm.

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17 13. The method recited in Claim 10 wherein said second thickness ranges
18 between about 6 nm and about 20 nm.

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20 14. The method recited in Claim 10 wherein said locating includes forming an
21 interface between first and second layers of said dielectric layer.

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23 15. The method recited in Claim 10 wherein said implanting includes
24 implanting said source and drain regions to a concentration of about $1.0\text{E}20$ atoms/cm³.

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2 16. The method recited in Claim 10 wherein said implanting includes
3 implanting a lightly doped region in each of said source and drain regions, wherein said
4 end of said gate and said second thickness are located over one of said lightly doped
5 regions.

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7 17. The method recited in Claim 16 wherein said implanting said lightly doped
8 region includes implanting to a concentration ranging between about $1.0\text{E}17$ atoms/cm³
9 and about $1.0\text{E}18$ atoms/cm³.

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11 18. The method recited in Claim 10 wherein said gate is a floating gate and
12 further including forming a control gate over said floating gate.

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1 19. An integrated circuit, comprising:
2 transistors formed over or in a semiconductor substrate;
3 memory cells, including:
4 source and drain regions located in said semiconductor substrate and
5 having similar doping profiles;
6 a channel region extending from said source region to said drain region;
7 a dielectric layer located over said source and drain regions and having
8 first and second thicknesses wherein said second thickness is substantially less
9 than said first thickness and is partially located over said channel region; and
10 a gate located over said dielectric layer wherein said second thickness is
11 located between an end of said gate and one of said source and drain regions;
12 and
13 interconnects connecting said transistors and said memory cells to form an
14 integrated circuit.

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16 20. The integrated circuit recited in Claim 19 wherein said memory cells are
17 EEPROM cells.

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19 21. The integrated circuit recited in Claim 19 wherein said first thickness
20 ranges between about 25 nm to about 50 nm and said second thickness ranges
21 between about 6 nm and about 20 nm.

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23 22. The integrated circuit recited in Claim 19 wherein a coupling ratio of each
24 of said memory cells is at least about 0.7.

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2 23. The integrated circuit recited in Claim 19 wherein said source and drain
3 regions each include a lightly doped region, wherein said end of gate and said second
4 thickness are located over one of said lightly doped regions.

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6 24. The integrated circuit recited in Claim 19 wherein said source and drain
7 regions include a doping concentration of about $1.0E20$ atoms/cm³ and said memory
8 cells further include lightly doped regions have a doping concentration ranging between
9 about $1.0E17$ atoms/cm³ and about $1.0E18$ atoms/cm³.

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